C-315: Study of multipliers in programmable logic devices

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Hardware multiplier is a major component in many computational and DSP systems which are implemented in Field Programmable Gate Arrays (FPGA). Since there are no universally accepted methods, designers often need to construct their own multipliers for the application in hand. Although there are various methods to perform multiplication operation in hardware, selection of a suitable multiplier not only improve the performance, but also save valuable configurable logic resources. In this work, a comparison of resource utilization and execution speed of several different types of multipliers in programmable logic devices is presented.

Two target hardware devices, a high density Spartan 3 FPGA and a low density XC4005XL FPGA were used. Pipelined and non-pipelined versions of Binary, Carry Save Array (CSA) and Cellular multipliers as well as the multiplier instantiated by the VHDL library by default were evaluated. In the case of the Spartan 3, the default multiplier was an embedded one which did not use any logic resources available for applications. Since XC4005XL chip has less configurable resources, only 4-bit and 8-bit multipliers were constructed while 4-bit, 8-bit and 18-bit multipliers were constructed in the Spartan 3 FPGA. It was found that the performance of the embedded multiplier available in the Spartan 3 was superior to all other multipliers. Next to the embedded multiplier, CSA multiplier was found to be the best in terms of resource utilization and speed. Further, the pipelined CSA multiplier performs approximately a factor of 2 faster than its non-pipelined version when a single stage pipelined is used. This speed could be further increased by inserting a few more pipelined stages.

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